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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,266	12/04/2003	Tetsuo Endoh	900-483	4564

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,266	ENDOH ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) 24-32 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1 page.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledge is made of applicants' claim for foreign priority base on an application 2002-354403 filed in Japan on 12/05/2002.

It is noted that Applicants have filled a certified copy of said application as required by U.S.C 119, which papers have been placed of record in the file.

Election/Restriction

Examiner confirms that Applicants elected to prosecute Claims 1-23 and have withdrawn Claims 24-32 without prejudice.

Information Disclosure Statement

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on **12/04/03** and made of record. The Japan patent document reference cited on the PTOL 1449 form have been considered, however, the cited U.S. Application No. (10/17,259) reference is invalid and therefore is not considered.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-32 of U.S. Patent No. 6,727,544. Although the conflicting claims are not identical, they are not patentably distinct from each other because the control gate and charge storage layer are formed entirely or partially around a sidewall of the island-like semiconductor layer (claim 1 of U.S. Patent No. 6,727,544 and claim 1 of present application), the insulation layer formed between the plurality of control gates of the plurality of memory cells for passing charges will be in a horizontal plane of the horizontal island-like semiconductor layer.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 6-19, 22-23 are rejected under 35 USC 102 (a) as being anticipated by Japan patent document No. 2877462, submitted by applicant as IDS.

Regarding claim 1, Japan patent document No. 2877462 discloses a semiconductor memory device comprising:

. a first conductivity type semiconductor substrate (P-Si);

. a plurality of memory cells 2 constituted of an island-like semiconductor layer which is formed on the substrate (Figs. 2A-2B, 4), and a charge storage layer 6 and a control gate 8 which are formed entirely or partially around a sidewall of the island-like semiconductor layer;

wherein the plurality of memory cells are disposed in series, the island-like semiconductor layer which constitutes the memory cells lies in a horizontal direction and an insulating film capable of passing charges is at least in a part of a plane of island-like semiconductor layer (see Figs. 2A-2B).

Regarding claim 6, Japan patent document No. 2877462 discloses the device in claim 1, wherein the memory cells 2 are electrically insulated from the substrate by a second conductivity type (source/drain, Figs. 2A-2B).

Regarding claims 7-9, Japan patent document No. 2877462 discloses the device in claim 1, wherein at least one memory cell insulated from other memory cell by a second conductivity type or by a depletion layer formed at a junction of the second conductivity type (source/drain, tunnel oxide film 5, Figs. 2A-2B).

Regarding claims 10-15, Japan patent document No. 2877462 discloses the method of claims 10-15: an impurity diffusion layer is formed on substrate and serves as

common wiring of memory cells, a plurality of island-line layers are arranged in matrix, wiring for reading out the state of a charge stored in memory cells, control gates are dislosed continuously in one direction to form a control gate line, plurality of wirings in a direction crossing the control gate line are connected to form a bit line, and gate electrode formed around the sidewall of island-like layer, and gate electrode is insulated from substrate or memory cells by second conductivity type, and part of corners of the island-like layer having a step shape so that a channel layers of memory cells are electrically connected (Specification, "background of prior art" and Figs. 2A-2B, 4, 10-11).

Regarding claims 16-17, Japan patent document No. 2877462 discloses the device of claims 1 and 11 and wherein control gates 8 are disposed closes to each other so that channel layers of the memory cells are electrically connected (See Figs. 2A-2B).

Regarding claims 18-19, Japan patent document No. 2877462 discloses the device of claims 1 and 11 and further disclose an electrode between control gate and gate electrode for connecting channels.

Regarding claims 22-23, Japan patent document No. 2877462 discloses the device of claim 1 and further discloses wherein a plurality of island-like layers are arranged in matrix and the width of the island-like layers or distance between island-like layers are smaller than the distance between and adjacent island-like layers in the same direction (specification, discussion of prior art, and Figs. 10-12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5, 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japan patent document No. 2877462, submitted by applicant as IDS.

Regarding claims 2-6, Japan patent document No. 2877462 discloses the cross-sectional areas of the island-like semiconductor layer are step by step small to the direction of the surface of the substrate (discuss of prior art in page 11) but fails to discloses the cross-sectional areas of the island-like semiconductor layer are step by step large or the same size to the direction of the surface of the substrate. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to obtain step by step large or the same size to the direction of the surface of the substrate because the size of the sectional areas between island-like layers would not change the functions or manner of the device.

Regarding claims 20-21, it is well known in the art that the control gate and gate electrode are made of the same material (conductive material) and the charge storage layer and gate electrode are made of same material (floating gate/gate electrode: conductive or polysilicon material).

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Forbes et al., U.S. Patent No. 6,512,695, also discloses the semiconductor device including limitations as recited in claims of present application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao P. Le
Examiner
Art Unit 2818